* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] Two or more signal terminals which deliver and receive various control signals including a refresh control signal, and the various signals which contain data and an address signal in a list between external circuits, The internal circuitry which performs writing of data, read-out, and refresh actuation according to the various signals transmitted including the memory cell array, the address selection circuit, and writing and a read-out control circuit, and outputs a predetermined signal, The refresh timer which answers the active level of the signal transmitted to the refresh control signal input edge, and generates a refresh demand signal to predetermined timing, The internal boundary scan control signal which is established corresponding to said each of two or more signal terminals, and contains a data shift clock is followed. At the time of the usual mode of operation The signal between signal terminals of the signal terminals of ****** plurality and other than the signal terminal corresponding to a refresh control signal and said internal circuitry and between said signal terminals corresponding to a refresh control signal and refresh control signal input edges of said refresh timer is transmitted. Cascade connection of the time of an internal static test mode is carried out one by one mutually, and two or more steps of shift registers are formed. The sequential shift by the side of the latter part of the data for a test from the outside, Two or more registers which perform the sequential shift by the side of the transfer to said internal circuitry of the signal of a predetermined stage, the incorporation to the predetermined stage of the signal from said internal circuitry, and the latter part of the signal incorporated by the list, and the signal output from the last stage, Said internal boundary scan control signal is followed. At the time of the usual mode of operation the refresh demand signal from said refresh timer It is the dynamic memory characterized by having the selection circuitry which chooses said data shift clock and is transmitted to the refresh demand signal input edge of said internal circuitry at the time of the signal shift action of said internal static test mode.
[Claim 2] The data for a test, static test mode setpoint signal, and test clock from the outside are received. The internal static test mode signal of active level, The data shift control signal which serves as active level to predetermined timing at the predetermined period of the active level of this internal static test mode signal, The data shift clock which serves as active level one by one during the period of the active level of this data shift control signal, Are behind from the internal test activation signal used as predetermined period active level, and this internal test activation signal during the period of the inactive level of said data shift control signal in the period of the active level of said internal static test mode signal. Active level The 1st input edge which prepares the boundary scan test control circuit which generates the becoming test activation result transfer control signal, and connects two or more registers of each with a corresponding signal terminal (or signal I/O edge where an internal circuitry corresponds), The 1st outgoing end linked to the signal I/O edge (or corresponding signal terminal) where said internal circuitry corresponds, The 2nd input edge which receives the output signal by the side of the preceding paragraph when forming a shift register (it is data from the outside if it is in a forefront stage), It has the 2nd (if it is in last stage, signal is outputted to the exterior) outgoing

end which transmits a signal to a latter-part side. Said internal static test mode signal transmits the signal of said 1st input edge to said 1st outgoing end at the period of inactive level. At the period of active level It synchronizes with said data shift clock at the period of the active level of said data shift control signal. Incorporate and hold the signal of said 2nd input edge, transmit to the 2nd outgoing end, and the active level of said internal test activation signal is answered at the period of the inactive level of this data shift control signal. Dynamic memory according to claim 1 made into the circuit which transmits said held signal to said 2nd outgoing end, answers the active level of said test activation result transfer control signal, incorporates and holds the signal of said 1st input edge, and is transmitted to said 2nd outgoing end.

[Claim 3] Dynamic memory according to claim 1 which is equipped with the self refresh control circuit which distinguishes that an internal circuitry is low supply voltage operating state, and generates an internal refresh control signal, and supplied said internal refresh control signal to the refresh control signal input edge of a refresh timer.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention relates to the dynamic memory which applied the boundary scan technique about dynamic memory.
[0002]
[Description of the Prior Art] In development and its manufacture of an electronic instrument, the test of an in circuit test, a function test, etc. is usually carried out to the mounting substrate which constitutes the electronic instrument in a predetermined phase, a module, IC, etc. However, diversification of the function of the electronic instrument which continues ceaseless, and an advancement affect the mounting substrate, a module, IC, etc., and result by the above-mentioned test technique in development and the test itself of a test tool not only taking long duration for a long period of time, but sufficient test becoming impossible and causing protraction of a development cycle and a manufacture period, the increase of cost, and lowering of dependability.
[0003] Then, the opportunity which is going to solve such a problem arises and the boundary scan technique aiming at development exchange of a test tool, exchange assistance of the test itself, and increase in efficiency is developed. In early stages of 1990 IEEE architecture Standard () 1149.1-1990." IEEE Standard Test Access a port -- and -- Boundary scan [IEEE Standard] Test Access Port and It was standardized as Boundary-ScanArchitecture."
[0004] The Van Dali scan technique is a test technique of preparing a data register between signal (these being hereafter called device) input/output terminals, such as a mounting substrate, and a module, IC, and an internal circuitry, carrying out cascade connection of these one by one, forming a register chain (shift register), controlling this register chain, and performing various kinds of tests.
[0005] The general example (the 1st example) which applied this boundary scan technique to dynamic memory is shown in drawing 4 .
[0006] This dynamic memory Various control signals including the refresh control signal REF, The various signals IN1-INm which contain data and an address signal in a list, two or more signal terminals TI1-TIm which deliver and receive OUT1-OUTn between external circuits, and TIr, TO1-TOn, The internal circuitry 1 which performs writing of data, read-out, and refresh actuation according to the various signals transmitted including the memory cell array, the address selection circuit, and writing and a read-out control circuit, and outputs a predetermined signal, The refresh timer 2 which answers the active level of the signal transmitted to the refresh control signal input edge, and generates the refresh demand signal RRQ to predetermined timing, The data TDI for a test, the static test mode setpoint signal TMS, and the test clock TCK from the outside are received. The internal static test mode signal ITM of active level, The data shift control signal SCN which changes with active level, inactive level, and active level to predetermined timing at the predetermined period of the active level of this internal static test mode signal ITM The data shift clock SCK which serves as active level one by one at the period of the active level of this data shift control signal SCN, In a list Are behind.

a period more nearly predetermined than the internal test activation signal ITE which serves as active level to predetermined timing at the period of the inactive level of the data shift control signal in the period of the active level of the internal static test mode signal ITM, and this internal test activation signal -- with active level The boundary scan test control circuit 3 which generates an internal boundary scan control signal including the becoming test activation result transfer control signal RTC (henceforth a BST control circuit), It is prepared corresponding to two or more terminals TI1-TIm, TIr and TO1 - each TOn. The above-mentioned internal boundary scan control signal is followed. When the internal static test mode signal ITM is the usual mode of operation of inactive level, the signal between the signal terminals TI1-TIm, and TO1-TOn and between the signal terminal TIr and the refresh control signal input edge of a refresh timer is transmitted. When the internal static test mode signal ITM is the internal static test mode of active level, cascade connection is carried out one by one mutually, and two or more steps of shift registers are formed. The sequential shift by the side of the latter part of the data for a test from the outside, In the transfer to the internal circuitry 1 of the signal of a predetermined stage, and a list, the incorporation to the predetermined stage of the signal from an internal circuitry, It has two or more registers RBI1 - RBIm which perform the sequential shift by the side of the latter part of the signal incorporated by the list, and the signal output from the last stage, RBIr, and the composition of having RBO1 - RBOn.

[0007] Moreover, as shown in drawing 5 , a register RBI1 - RBIm, RBIr, and RBO1 - RBOn, respectively The 1st input edge PI linked to a corresponding signal terminal (or signal I/O edge where an internal circuitry 1 corresponds) The 1st outgoing end RPO linked to the signal I/O edge (or corresponding signal terminal) where an internal circuitry 1 corresponds, The 2nd input edge SI which receives the output signal by the side of the preceding paragraph when forming a shift register (it is the data TPI for a test from the outside if it is in a forefront stage) The 2nd (if it is in last stage, signal is outputted to the exterior) outgoing end RPO which transmits a signal to a latter-part side, The selector SL 1 which chooses one side of the signal of the 1st and 2nd input edge PI and SI according to the data shift control signal SCN D-type-flip-flop FF1 which latches the output signal of a selector SL 1 according to the data shift clock SCK and the internal test-result transfer control signal RTC, and is outputted to the 2nd outgoing end SO, D-type-flip-flop FF2 which latches and outputs the output signal of D-type-flip-flop FF1 according to the internal test activation signal ITE, It has the selector SL 2 which chooses either the signal of the 1st input edge, or the output signal of D-type-flip-flop FF2 according to the internal static test mode signal ITM, and is outputted from the 1st outgoing end PRO. The internal static test mode signal ITM transmits the signal of the 1st input edge PI to the 1st outgoing end RPO at the period of inactive level. At the period of active level It synchronizes with the data shift clock SCK at the period of the active level of the data shift control signal SCN. Incorporate and hold the signal of the 2nd input edge SI, transmit to the 2nd outgoing end SO, and the active level of the internal test activation signal ITE is answered at the period of the inactive level of this data shift control signal SCN. It has composition which transmits the held signal to the 2nd outgoing end SO, answers the active level of the test activation result transfer control signal RTC, incorporates and holds the signal of the 1st input edge PI, and is transmitted to the 2nd outgoing end SO.

[0008] Next, about actuation of this dynamic memory, the timing chart of each part signal shown in drawing 6 is referred to collectively and explained.

[0009] first, when the internal static test mode signal ITM is the inactive level of a low The signal of the 1st input edge PI of each register is transmitted to the 1st outgoing end RPO by the selector SL 2. The signal (IN1-INm) of the signal terminals TI1-TIm is transmitted to an internal circuitry 1, the output signal of an internal circuitry 1 is transmitted to the signal terminals TO1-TOn, an internal circuitry 1 performs the usual write-in actuation and read-out actuation, and the result is outputted from the signal terminals TO1-TOm. Moreover, the refresh control signal REF of the signal terminal TIr is transmitted to the refresh timer 2, and this refresh timer 2 answers the active level of the refresh control signal REF, generates the

sequential refresh demand signal RRQ, and transmits it to an internal circuitry 1. And an internal circuitry 1 performs refresh actuation according to this refresh demand signal RRQ.
[0010] Next, the internal static test mode signal ITM explains actuation of the internal static test mode of active level (high level).
[0011] first, the data shift control signal SCN -- signal terminal TI1- for [various] a signal input -- while between TIm, TIr, and registers RBI1 - RBIm(s) and RBIr(s) and between the signal outgoing end of an internal circuitry 1, and registers RBO1 - RBOn(s) are separated, cascade connection of these registers is carried out one by one by the 2nd input edge SI and the 2nd outgoing end SO, and they form two or more steps of shift registers. And synchronizing with the data shift clock SCK in which the active level of the data shift control signal SCN carries out sequential generating in a period, the data TDI for a test from the input edge of the register (this example ROIr) of a forefront stage are shifted to a latter-part side one by one, when it is transmitted to the register with which the data for these tests correspond and is held, the data shift control signal SCN serves as inactive level, and generating of the data shift clock SCK stops it. Therefore, between registers is separated and between a register and an internal circuitry, and a refresh timer is connected between a signal terminal and a register.
[0012] The active level of the internal test activation signal ITM is answered first, and the data (data IN1-INm held at D-type-flip-flop FF1) held at the predetermined register (this example RBI1 - RBIm) are incorporated by D-type-flip-flop FF2, it is transmitted to an internal circuitry 1 through a selector SL 2, and actuation predetermined by the internal circuitry 1 is performed at the period of the inactive level of this data shift control signal SCN. And the active level of the internal test activation result transfer control signal RTC is answered, and the output signal (output data) of an internal circuitry 1 is incorporated and held at D-type-flip-flop FF1 of a predetermined register (this example RBO1 - RBOn).
[0013] If the data shift control signal SCN is again set to active level, a register RBI1 - RBIm, RBIr, and RBO1 - RBOn form two or more steps of shift registers, and synchronizing with the data shift clock which carries out sequential generating, the held data (signal) will be shifted to a latter-part side one by one, and will be outputted to the exterior from the outgoing end of the register RBOn of the last stage (TDO).
[0014] In this way, actuation of an internal circuitry 1 can be tested regardless of the signal terminals TI1-TIm and the signal of TIr, TO1-TOn.
[0015] Although this example explained the dynamic memory in the case of inputting the refresh control signal REF from the outside, and performing refresh actuation, in the dynamic memory which operates with low supply voltage by battery backup etc., and has a mode of operation aiming at data-hold, supply voltage is detected, an internal refresh control signal is generated, and a refresh timer is operated. The example (the 2nd example) which applied the boundary scan technique to such dynamic memory is shown in drawing 7 .
[0016] If the point that this dynamic memory is different from the dynamic memory shown in drawing 4 falls from the level (it is 2V when the usual supply voltage is set to 5V) to which supply voltage was set beforehand, it will be equipped with the self refresh control circuit 5 which generates the internal refresh control signal IREF used as active level, and it is in the point which replaced the signal to the refresh control signal input edge of the refresh timer 2 with the refresh control signal REF from the outside, and made it an internal refresh control signal IREF.
[0017] In this dynamic memory, if supply voltage falls from predetermined level, the refresh demand signal RRQ will be supplied to an internal circuitry 1 from the refresh timer 2, and refresh actuation will be performed within an internal circuitry 1. Other actuation is the same as that of the 1st example.
[0018]
[Problem(s) to be Solved by the Invention] The conventional dynamic memory mentioned above in the 1st example At the time of an internal static test mode, at the period of the active level of the beginning of the data shift control signal SCN Separate between the signal terminal for

[various] a signal input, and response registers, and between the signal outgoing end of an internal circuitry 1, and response registers, carry out cascade connection of between registers, and it considers as two or more steps of shift registers. Shift the data for a test to a latter-part side one by one with the data shift clock SCK, and it is made to set up and hold to D-type-flip-flop FF1 of a predetermined register. Between registers is separated at the period of the next inactive level of the data shift control signal SCN, and between a signal terminal and a register and between a register and an internal circuitry 1, and the refresh timer 2 are connected. With the internal test activation signal ITE Incorporate the data currently held at D-type-flip-flop FF1 of a predetermined register to D-type-flip-flop FF2, and it transmits to an internal circuitry 1. Make an internal circuitry 1 perform predetermined actuation, and incorporate the result to D-type-flip-flop FF1 of a predetermined register with the internal test activation result transfer control signal RTC, and it is held. Cascade connection of between registers is again carried out to the period of the next active level of the data shift control signal SCN, and it considers as two or more steps of shift registers. With the data shift clock SCK Since it has composition which shifts to a latter-part side the data held at the predetermined register one by one, and is outputted from the last stage The refresh control signal REF from the outside does not make it transmit to the refresh timer 2 during the period of an internal static test mode. Moreover, in order to incorporate the data for a test set as D-type-flip-flop FF1 to D-type-flip-flop FF2 with the internal test activation signal ITE and to transmit to the refresh timer 2, If the level of the signal incorporated to this D-type-flip-flop FF2 is the inactive level of the refresh control signal REF, and corresponding level The refresh control signal input edge of the refresh timer 2 It is still inactive level until it is set to active level with the internal test activation signal ITE. The refresh demand signal RRQ is not outputted from the refresh timer 2, refresh actuation by the internal circuitry 1 is not performed, but there is a trouble that stored data will disappear.

[0019] Moreover, in the 2nd example, since the refresh demand signal RRQ is not outputted from the refresh timer 2 unless it falls from the level to which supply voltage was set beforehand, when an internal static test mode is performed with the usual supply voltage, the refresh demand signal RRQ does not occur but there is a trouble that stored data will disappear as well as the 1st example.

[0020] The object of this invention is to offer the dynamic memory which can be prevented from disappearing stored data, whether control of refresh actuation is based on a control signal from the outside or is based on an internal control signal, and when an internal static test mode is performed with the usual supply voltage.

[0021]

[Means for Solving the Problem] Two or more signal terminals with which the dynamic memory of this invention delivers and receives various control signals including a refresh control signal, and the various signals which contain data and an address signal in a list between external circuits, The internal circuitry which performs writing of data, read-out, and refresh actuation according to the various signals transmitted including the memory cell array, the address selection circuit, and writing and a read-out control circuit, and outputs a predetermined signal, The refresh timer which answers the active level of the signal transmitted to the refresh control signal input edge, and generates a refresh demand signal to predetermined timing, The internal boundary scan control signal which is established corresponding to said each of two or more signal terminals, and contains a data shift clock is followed. At the time of the usual mode of operation The signal between signal terminals of the signal terminals of ****** plurality and other than the signal terminal corresponding to a refresh control signal and said internal circuitry and between said signal terminals corresponding to a refresh control signal and refresh control signal input edges of said refresh timer is transmitted. Cascade connection of the time of an internal static test mode is carried out one by one mutually, and two or more steps of shift registers are formed. The sequential shift by the side of the latter part of the data for a test from the outside, Two or more registers which perform the sequential shift by the side of the transfer to said internal circuitry of the signal of a predetermined stage, the incorporation to

the predetermined stage of the signal from said internal circuitry, and the latter part of the signal incorporated by the list, and the signal output from the last stage, Said internal boundary scan control signal is followed. At the time of the usual mode of operation the refresh demand signal from said refresh timer It has the selection circuitry which chooses said data shift clock and is transmitted to the refresh demand signal input edge of said internal circuitry at the time of the signal shift action of said internal static test mode.

[0022] The data for a test, static test mode setpoint signal, and test clock from the outside are received. Moreover, the internal static test mode signal of active level, The data shift control signal which serves as active level to predetermined timing at the predetermined period of the active level of this internal static test mode signal, The data shift clock which serves as active level one by one during the period of the active level of this data shift control signal, Are behind from the internal test activation signal used as predetermined period active level, and this internal test activation signal during the period of the inactive level of said data shift control signal in the period of the active level of said internal static test mode signal. Active level The 1st input edge which prepares the boundary scan test control circuit which generates the becoming test activation result transfer control signal, and connects two or more registers of each with a corresponding signal terminal (or signal I/O edge where an internal circuitry corresponds), The 1st outgoing end linked to the signal I/O edge (or corresponding signal terminal) where said internal circuitry corresponds, The 2nd input edge which receives the output signal by the side of the preceding paragraph when forming a shift register (it is data from the outside if it is in a forefront stage), It has the 2nd (if it is in last stage, signal is outputted to the exterior) outgoing end which transmits a signal to a latter-part side. Said internal static test mode signal transmits the signal of said 1st input edge to said 1st outgoing end at the period of inactive level. At the period of active level It synchronizes with said data shift clock at the period of the active level of said data shift control signal. Incorporate and hold the signal of said 2nd input edge, transmit to the 2nd outgoing end, and the active level of said internal test activation signal is answered at the period of the inactive level of this data shift control signal. It is constituted as a circuit which transmits said held signal to said 2nd outgoing end, answers the active level of said test activation result transfer control signal, incorporates and holds the signal of said 1st input edge, and is transmitted to said 2nd outgoing end.

[0023] Moreover, it has the self refresh control circuit which distinguishes that an internal circuitry is low supply voltage operating state, and generates an internal refresh control signal, and has the configuration which supplied said internal refresh control signal to the refresh control signal input edge of a refresh timer.

[0024]

[Example] Next, the example of this invention is explained with reference to a drawing.

[0025] Drawing 1 is the block diagram showing the 1st example of this invention.

[0026] The point that this example is different from the conventional dynamic memory shown in drawing 4 chooses the refresh demand signal outputted from the refresh timer 2, when the data shift control signal SCN is inactive level, and it is in the point of having formed the selector 4 which chooses the data shift clock SCK and is transmitted to the refresh demand signal input edge of an internal circuitry 1, at the time of active level.

[0027] Next, actuation of this example is explained. Drawing 2 is the timing chart of each part signal for explaining actuation of this example.

[0028] First, when the internal static test mode signal ITM is the usual mode of operation of inactive level (low), it is inactive level (low), and the data shift control signal SCN chooses the refresh demand signal TRQ outputted from the refresh timer 2, and transmits a selector 4 to an internal circuitry 1 as a refresh demand signal RRQ. Consequently, refresh actuation of an internal circuitry 1 is performed. This actuation is the same as the conventional example shown in drawing 4 and drawing 6 .

[0029] Next, when the internal static test mode signal ITM is the internal static test mode of active level (high level), the active level (high level) of the data shift control signal SCN is

answered, and a selector 4 chooses the data shift clock SCK, and transmits it to an internal circuitry 1 as a refresh demand signal RRQ. Consequently, refresh actuation of an internal circuitry 1 is performed. Since the data shift control signal SCN serves as active level at the time of the data shift when setting the data for a test as each register, and the signal (data) shift which outputs the signal of the test result after test activation of an internal circuitry 1 to the exterior in order to perform the test of an internal circuitry 1, even when the number of signal terminals increases and a data shift takes long duration, stored data does not disappear.

[0030] Drawing 3 is the block diagram showing the 2nd example of this invention. It is the point which this example applied this invention to the 2nd conventional example shown in drawing 7 , and the point of difference with the 1st example replaced the signal to the refresh control signal input edge of the refresh timer 2 with the refresh control signal REF from the signal terminal TIr and Register RBIr, and was made into the internal refresh control signal IREF from the self refresh control circuit 5.

[0031] Since the self refresh control circuit 5 does not make the internal refresh control signal IREF active level unless supply voltage falls from 2V, when an internal static test mode is performed with the usual supply voltage (for example, 5V), the refresh demand signal TRQ is not outputted from the refresh timer 2. However, in this example, even in this case, since the data shift clock SCK is transmitted to an internal circuitry 1 by the selector 4 as a refresh demand signal RRQ, refresh actuation of an internal circuitry 1 is performed and stored data does not disappear.

[0032]

[Effect of the Invention] As explained above, this invention supplies the refresh demand signal outputted from a refresh timer at the time of the usual mode of operation to an internal circuitry. At the time of an internal static test mode When setting the data for a test as each register for internal test activation Since it considered as the configuration supplied to an internal circuitry by making into a refresh demand signal the data shift clock which performs the data shift when outputting to the exterior the test result incorporated by each register after a ** data shift and internal test activation Even if control of refresh actuation is based on a control signal from the outside Moreover, even if based on the internal control signal which detects the level of supply voltage and is generated, when an internal static test mode is performed with the usual supply voltage, it is effective in the ability to prevent stored data from disappearing.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the 1st example of this invention.
[Drawing 2] It is the timing chart of each part signal for explaining actuation of the example shown in drawing 1 .
[Drawing 3] It is the block diagram showing the 2nd example of this invention.
[Drawing 4] It is the block diagram showing the 1st example of the conventional dynamic memory.
[Drawing 5] It is the circuit diagram showing the example of the register of the dynamic memory shown in drawing 5 .
[Drawing 6] It is the timing chart of each part signal for explaining actuation of the dynamic memory shown in drawing 4 .
[Drawing 7] It is the block diagram showing the 2nd example of the conventional dynamic memory.
[Description of Notations]
1 Internal Circuitry
2 Refresh Timer
3 BST Control Circuit
4 Selector
5 Self Refresh Control Circuit
FF1, FF2 D type flip-flop
RBI1 - RBIm, RBIr, RBO1 - RBOn Register
SL1, SL2 Selector
TI1-TIm, TIrTO1-TOn Signal terminal

[Translation done.]

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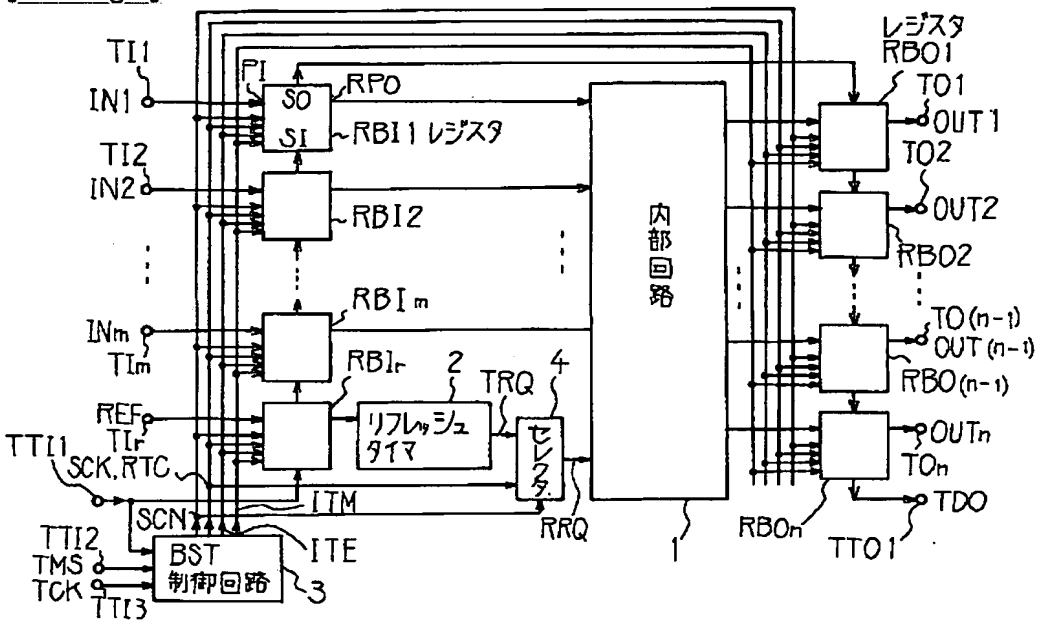
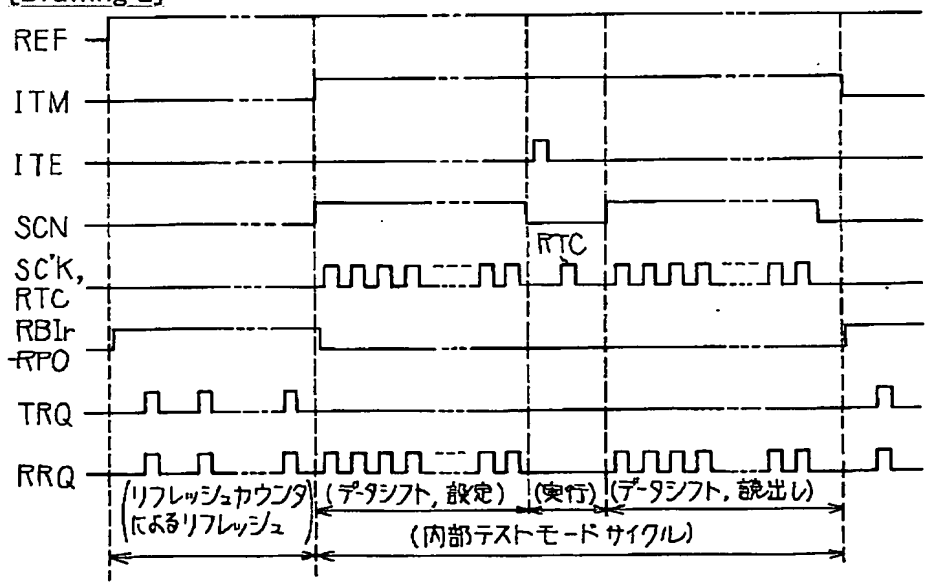
DRAWINGS

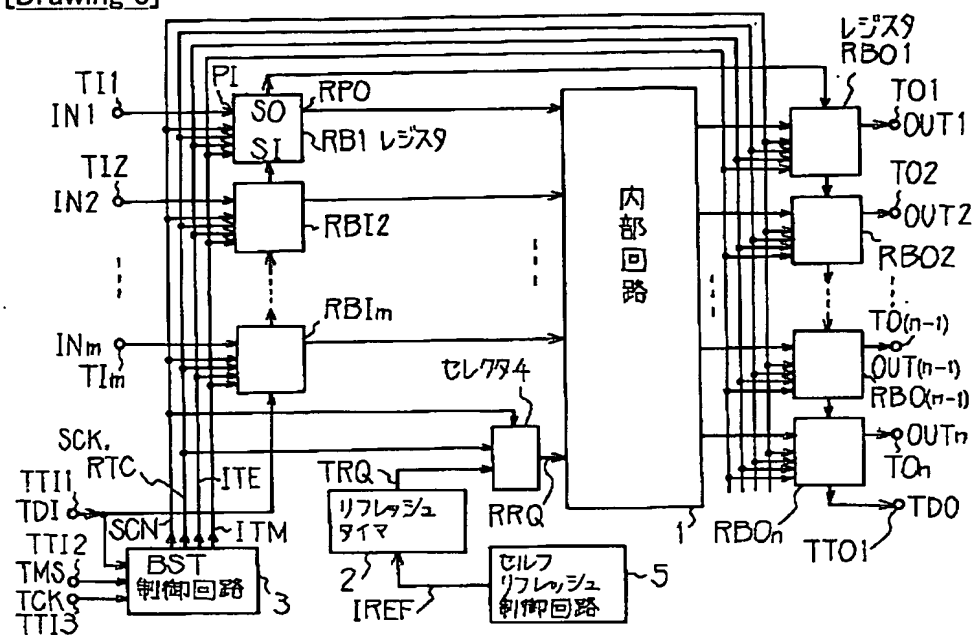
[Drawing 1]



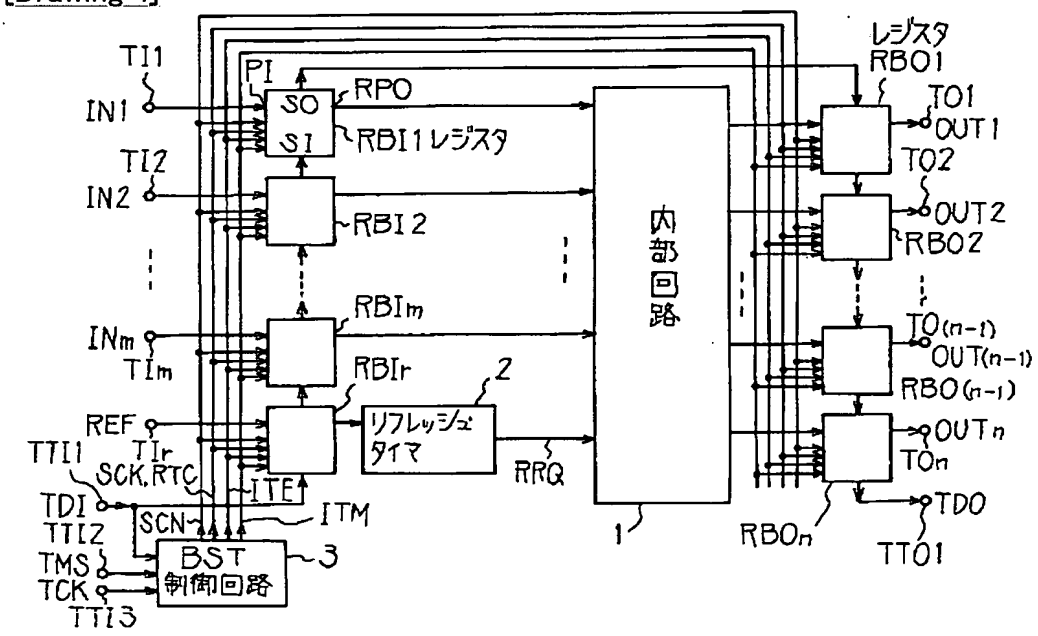
[Drawing 2]



[Drawing 3]



[Drawing 4]



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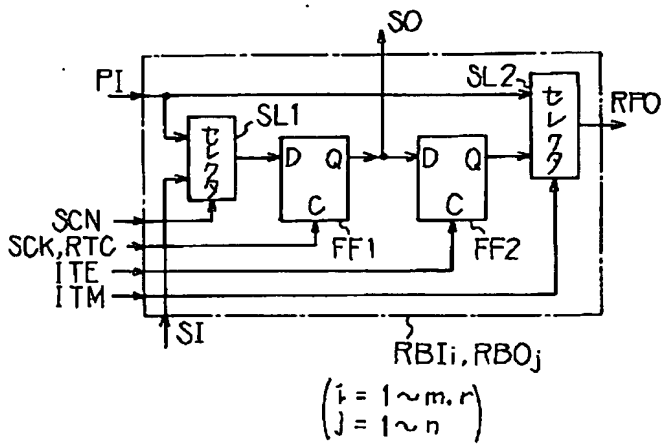
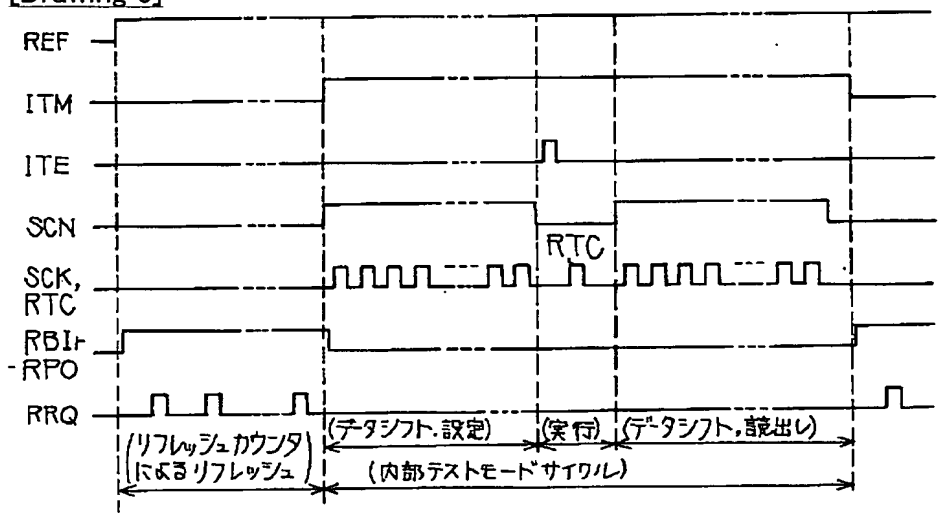
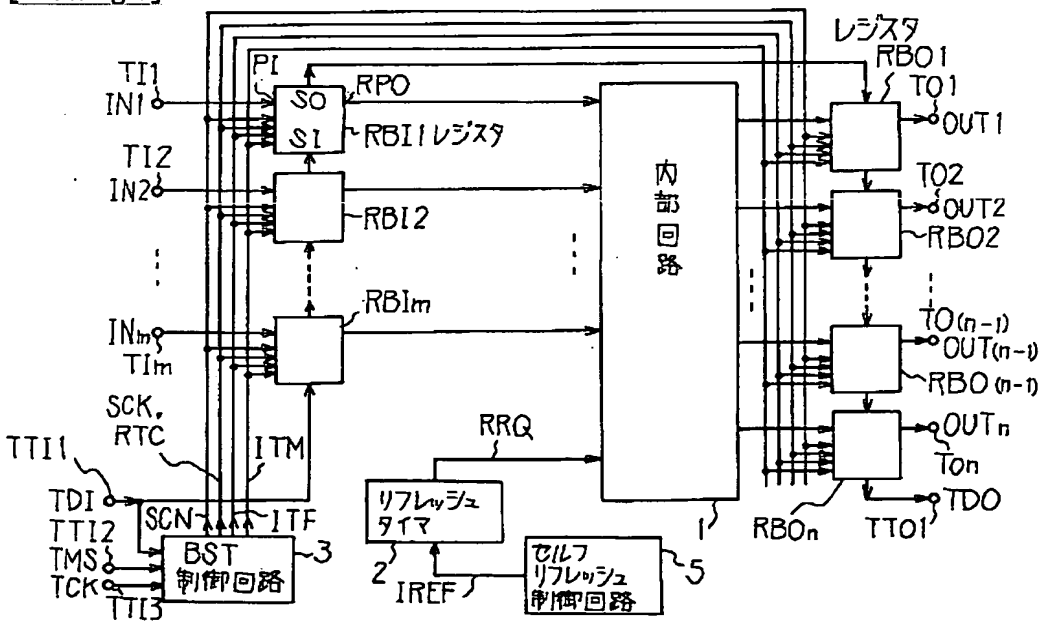


FF1, FF2 … D型フリップフロップ

[Drawing 6]



[Drawing 7]



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